## ABSTRACT OF THE DISCLOSURE

A method and architecture accesses a unified memory in a micro-processing system having a two-phase clock. The unified memory is accessed during a first instruction cycle. When a program code discontinuity is encountered, the unified memory is accessed a first time during an instruction cycle with a dummy access. The unified memory is accessed a second time during the instruction cycle when a program code discontinuity is encountered with either a data access, as in the case of a last instruction of a loop, or an instruction access, as in the case of a jump instruction.